

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YASUHIRO KOYAMA AND HIROSHI ISHIHARA

Appeal No. 95-3455
Application 07/945,902¹

HEARD: 13 JANUARY 1999

Before METZ, JOHN DOUGLAS SMITH and PAK, Administrative Patent Judges.

METZ, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134 from the examiner's refusal to allow claims 3 and 5 through 7, all the claims remaining in the application.

THE INVENTION

¹ Application for patent filed September 17, 1992.

The claimed invention is directed to a method for forming a non-volatile memory having a floating gate electrode. Floating gate electrodes are useful in re-writable, non-volatile memory devices such as the so-called EPROM's (electrically programmable read only memory devices). The floating gate electrode is so-named because an insulating tunnel oxide is sandwiched between the gate electrode and the underlying silicon substrate. Thus, charges flowing in the underlying substrate through the tunnel oxide into the floating gate electrode are prevented from flowing back by the tunnel oxide insulation.

Claim 6 is reproduced below for a more facile understanding of appellants' invention.

Claim 6. A method for forming a non-volatile memory having a floating gate electrode comprising the steps of:

(a) forming a tunnel oxide layer used for writing information on a silicon substrate,

(b) forming a polysilicon layer on the tunnel oxide layer,

(c) forming a tungsten silicide layer over the polysilicon layer with a chemical vapor deposition using WF_6 gas reduced with a SiH_2Cl_2 gas at a temperature in the range of 500 to 600°C, and the fluorine content in the resulting

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tungsten silicide layer being 1×10^{20} atom/cm³ or less, and

(d) patterning the polysilicon layer and the tungsten silicide layer by etching to make a floating gate.

THE PRIOR ART

The references of record which are being relied on by the examiner as evidence of obviousness are²:

Hillman et al. (Hillman)	4,966,869	Oct.
30, 1990		
Itoh	5,120,673	Jun.
9, 1992 ³		
Mitchell	5,156,990	Oct. 20, 1992 ⁴
Kume et al. (Kume)	5,188,976	Feb. 23, 1993 ⁵

A reference cited by appellants as evidence of non-

² In his Answer, the examiner has withdrawn his reliance on the disclosure of the U.S. patent to Wada.

³ Application filed on January 25, 1991.

⁴ A division of U.S. Application 07/889,454, filed on July 23, 1986, now U.S. Patent Number 4,979,005 issued December 18, 1990.

⁵ Application filed on July 9, 1991.

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obviousness is:

"Evaluation of CVD WSix Film Employing SiH_2Cl_2 " by Koyama et al., published from the "Proceedings of the 41st Symposium on Semiconductors and Integrated Circuits Technology" in Tokyo, Japan in December 1991.

Two references relied on by the Board under 37 C.F.R.

§ 1.196(b) as evidence of obviousness are:

Price et al. (Price'343)	4,692,343	Sep. 8,
1987		
Price et al. (Price'474)	4,737,474	Apr. 12, 1988

THE REJECTIONS

Claims 3 and 5 through 7 stand rejected as failing to comply with the "written description" requirement of 35 U.S.C. § 112, first paragraph. Claims 3 and 5 through 7 stand rejected as

being unpatentable under 35 U.S.C. § 103 from the disclosure of Kume considered with Mitchell or Itoh, considered with Hillman. We reverse.

THE REJECTION UNDER 35 U.S.C. § 112

We agree with appellants that it is difficult to determine exactly on which section of 35 U.S.C. § 112 the examiner has relied to reject appellants' claims. As the

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court made clear in its decision in In re Rasmussen, 650 F.2d 1212, 1214-15, 211 USPQ 323, 325-26 (CCPA 1981), Section 132 of Title 35 prohibits the introduction of "new matter" into the disclosure of an application. Section 112, first paragraph, requires that claim language be described and enabled in the specification. Thus, an amended claim thought to lack an adequate "written description" in the original disclosure should be rejected under 35 U.S.C. § 112, first paragraph.

Although the examiner's rejection before us is stated to be under the first paragraph of 35 U.S.C. § 112, it is founded on the examiner's objection to the specification because "as originally filed, [the specification] does not provide support for the invention as is now claimed." (page 3 of the Answer). However, we observe that there have been no changes made to nor subject matter added to the disclosure on pages 5 and 6 of the specification on which disclosure the examiner relies for the

proposition that insulating is a required step in forming appellants' gate electrode. Thus, the examiner's "new matter"

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objection is poorly founded.

On page 7 of his Answer, the examiner explains the rejection under Section 112 as founded on his position that:

the specification teaches that the only way to form a floating gate electrode is to coat the etched surface with an insulating layer. The examiner contends that the specification does not disclose forming a floating gate electrode without an insulating layer and that the insulating layer appears to be a critical feature of the invention.

Thus, it appears to be the examiner's position that because step "(d)" of claim 6 recites making a floating gate only by patterning by etching the polysilicon layer and tungsten silicide layer without insulating the etched layer, step "(d)" of claim 6, and claim 6 itself is not for the invention described in appellants' original disclosure. Stated another way, the examiner has interpreted appellants' disclosure as requiring insulating after etching to make a gate electrode. But this would seem to raise a question under 35 U.S.C. § 112, second paragraph, on the ground that appellants have failed to present a claim for that which they believe to be their invention or a question of enablement under the first paragraph of 35 U.S.C.

§ 112.

We agree with appellants that a claim is not intended to be a blueprint or a production specification. See In re Gay, 309 F.2d 769, 774, 135 USPQ 311, 316 (CCPA 1962). Rather, the question to be resolved here concerning the "written description" requirement of 35 U.S.C. § 112 is whether or not appellants' original disclosure reasonably conveyed that they were possessed of, as of their filing date, the invention later claimed by them. The primary inquiry into satisfaction of the "written description" requirement is factual and depends on the nature of the invention and the amount of knowledge imparted to those skilled in the art by the disclosure. In re Wertheim, 541 F.2d 257, 262, 191 USPQ 90, 96 (CCPA 1976).

As correctly noted by appellants, the steps positively recited in claim 6, that is, patterning the polysilicon layer and the tungsten silicide layer by etching are described in appellants' original disclosure. Moreover, as appellants have noted, claim 6 is a "comprising" claim and, thus, is open to the inclusion of other steps and ingredients, even steps and

ingredients not disclosed by appellants. Thus, the narrow question before us resolves to whether or not a person of ordinary skill in the art, given appellants' original disclosure, would have understood that an additional step of coating the etched layers of polysilicon and tungsten silicide with an

insulating layer was required "to make a floating gate" as the language of claim 6 requires.

As we have stated above, as a "comprising" claim, claim 6 is open to the inclusion of additional steps and ingredients, even steps and ingredients neither contemplated nor disclosed by appellants. Thus, although claim 6 recites only four steps necessary to form a non-volatile memory, we take official notice of the fact that in real practice there are numerous preparatory steps, process steps and finishing steps required to form a "non-volatile memory having a floating gate electrode" which steps are not recited in claim 6. Therefore, in order to sustain the examiner's position, we must be directed to some evidence that a person of ordinary skill in the art would have recognized appellants' recited step "(d)"

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as inadequate to "make a floating gate." In our opinion, there is no such evidence of record.

Indeed, the examiner's only basis for so-concluding is his conclusion that "there is no support in the specification for forming a floating gate electrode without an insulating layer" (page 9 of the Answer). That conclusion is, on its face, factually erroneous. On page 1 of the specification, forming a floating gate electrode by laminating on a silicon substrate either polysilicon or polysilicon followed by a tungsten silicide layer with a tunnel oxide layer sandwiched between is described. No step of coating the laminate with an insulating layer is described therein. Except for the use of dichlorosilane instead of silane, this disclosure essentially tracks verbatim original claim 1 of appellants' application. Original claims constitute part of the original disclosure of a patent application. See In re Gardner, 475 F.2d 1389, 1391, 177 USPQ 396, 397 (CCPA 1973); In re Anderson, 471 F.2d 1237, 1238-39, 176 USPQ 331, 332 (CCPA 1973); In re Myers, 410 F.2d 420, 427, 161 USPQ 668, 673 (CCPA 1969).

For all the above reasons, we find that the examiner has failed to factually establish any basis for concluding that

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the steps recited in step "(d)" of claim 6 are not described in appellants' original disclosure. Nor has the examiner factually established that a person of ordinary skill in the art of semiconductor manufacture would have been unable to practice appellants' process described in claim 6 without resort to "undue" experimentation. Accordingly, we reverse the rejection under 35 U.S.C. § 112, first paragraph.

Our review of the Section 112 issue has left us with the impression that the examiner's rejection of claim 6 could have properly been founded on the second paragraph of Section 112 and that such a rejection could have been sustained.

Nevertheless, we are mindful that appellants have filed an amendment to claim 6 which, in our view, removes all issues under Section 112 with respect to claim 6. Thus, we exercise our authority under

37 C.F.R. § 1.196(c) and direct the examiner to enter appellants' amendment filed on July 6, 1994 (Paper Number 9).

THE REJECTION UNDER 35 U.S.C. § 103

It is by now fundamental that when rejecting the subject matter claimed by an appellant under 35 U.S.C. § 103 the examiner is charged with the initial burden of making out a

prima facie case of obviousness. In our view, the examiner has failed to analyze appellants' claims vis-à-vis the prior art in the manner required in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966).

While the examiner has relied on Kume as the primary or basic reference in his rejection, the examiner agrees with appellants' argument that Kume fails to disclose a laminated floating gate electrode formed of polysilicon and that Kume's floating gate electrode is formed solely from polycrystalline silicon (see the Answer, page 9). Nonetheless, the examiner notes that the rejection is over a combination of references not over Kume, alone. The examiner also agrees "in principle" with appellants' argument that the gate electrode of Kume lacks an underlying tunnel oxide.

The examiner also agrees "in part" with appellants' characterization of the Mitchell and Itoh references as not requiring a laminated gate electrode formed from tungsten silicide over polysilicon and as being directed to a field effect transistor (FET) not a floating gate electrode, respectively. Likewise, the examiner agrees with appellants' characterization of Hillman as not being directed to a memory

cell or a floating gate electrode and as not teaching that dichlorosilane may be combined with tungsten hexafluoride to form a floating gate electrode.

Indeed, appellants' only characterization of the prior art with which the examiner totally disagrees is that Hillman fails to recognize that fluorine contaminants in tungsten silicide lead to deterioration of the tunnel oxide. The examiner posits that since none of the prior art on which the examiner relies discloses that fluorine contamination in the tungsten silicide layer leads to breakdown of the tunnel oxide, it is mere speculation by appellants that such a phenomenon exists.

The examiner also observes that, in his opinion, there is no recitation in the claims of a laminated, floating gate electrode. We certainly agree that appellants' claimed method does not use the language "laminated floating gate electrode" *in ipsimis verbis*. However, we find it difficult to understand the examiner's basis for concluding that first forming a tunnel oxide layer on silicon and thereafter forming a layer of polysilicon of the tunnel oxide and then a tungsten silicide layer over the polysilicon would not yield a

laminated floating gate electrode. Thus, the basis for examiner's conclusion that "any arguments establishing criticality of a laminated floating gate electrode is irrelevant" (page 10 of the Answer) also escapes us and erroneously fails to properly consider the claimed method.

While the logic of certain positions taken by the examiner in his Answer are inescapable, the flaw in the examiner's positions reside in the fact that there is no motivation found in the prior art to do what the examiner suggests. Rather, we find the examiner has relied on appellants' disclosure for evidence of motivation and equivalence. Thus, on this record, the examiner has not factually established the basis upon which he has predicated the requisite motivation for the proposed combination of references. In re Laskowski, 871 F.2d 115, 117, 10 USPQ2d 1397, 1398 (Fed. Cir 1989); Smithkline Diagnostics Inc. v. Helena Laboratories Corp., 859 F.2d 878, 887, 8 USPQ2d 1468, 1475 (Fed. Cir 1988). Moreover, there is scant analysis of what appellants' claims recite or require in the examiner's statement of his rejection. Analysis of the claims is the starting point for the analysis required in Graham v. John

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Deere, *supra*.

Based upon the totality of the evidence before us, it is our judgment that the examiner has retrospectively concluded that appellants' invention would have been obvious using appellants' claims as a blueprint for his conclusions. Accordingly, the decision of the examiner is **REVERSED**.

REJECTION UNDER 37 C.F.R. § 1.196(b)

Pursuant to our authority under 37 C.F.R. § 1.196(b), we enter the following new ground of rejection.

Claims 3 and 5 through 7 are rejected under 35 U.S.C. § 103, as being unpatentable from appellants' admissions at page 1, lines 17 through 24 considered with any one of Hillman, Price'343, Price'474 or Koyama et al.

THE PRIOR ART

As we have stated above, the new ground of rejection is founded, in part, on what we have characterized as "appellants' admissions". Rejections founded on evidence of what appellants have conceded to be prior art with respect to their claimed invention is not without precedent. See In re

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Nomiya, 509 F.2d 566, 570-71, 184 USPQ 607, 611 (CCPA 1975).

Accordingly, we shall first determine the scope and content of "appellants' admissions."

Under the caption "Description of the Prior Art" on page 1 of their specification, appellants recite at lines 17 through 24 that:

As a method for forming a floating gate electrode formed by laminating a polysilicon layer or by alternately laminating a polysilicon and a tungsten silicide layer with a tunnel oxide sandwiched between said substrate and said polysilicon layer, known is a method wherein a tungsten silicide layer is laminated on a polysilicon layer with a CVD technique of reducing WF_6 gas with SiH_4 gas at 300°C to 400°C under reduced pressure.

At oral hearing, appellants' legal representative was asked if the salient step in the claimed process *vis-à-vis* the prior art referenced in their specification at page 1 was the use in step "(c)" of claim 6 of dichlorosilane instead of silane. Appellants' legal representative answered in the affirmative. See also page 2 of appellants' brief, lines 12 and 13. Thus, claim 6 (unamended) differs from the admitted prior art process only in requiring dichlorosilane as the reducing gas for tungsten hexafluoride rather than silane as the reducing

gas.

Hillman is directed to the manufacture of semiconductor devices using chemical vapor deposition (CVD) of tungsten silicide by the reduction of tungsten hexafluoride by silane gases (column 1, lines 5 through 9). At column 1, lines 14 through 16, tungsten silicide is described as particularly useful in the manufacture of gate metallizations wherein a low resistivity tungsten silicide layer is formed on a polysilicon layer. In the ensuing discussion at column 1, lines 21 through 50, Hillman discloses, *inter alia*, that using dichlorosilane leads to cleaner deposition chambers and cites voluminous prior

art said to describe "[t]he use of dichlorosilane instead of silane".

Price'343 discloses that when using plasma reactors for depositing silicon, silane is known to deposit silicon everywhere once a minimum temperature is achieved while silicon tetrachloride will not deposit silicon when used alone. Dichlorosilane is described as having properties intermediate silane and silicon tetrachloride. See column 1,

lines 8 through 27. At column 9, lines 5 through 16, an example of depositing tungsten silicide from a mixture of dichlorosilane and tungsten hexafluoride is described. A rapid, efficient deposition is obtained. See also claim 2 which claims the use of tungsten hexafluoride and dichlorosilane.

Price'474 discloses the manufacture of semiconductor devices having a silicide/silicon bond (column 1, lines 5 through 7). Improved metal gate systems for MOS devices are achieved by depositing an intermediate amorphous silicon layer on polycrystalline silicon with a silicide such as tungsten silicide deposited over the amorphous silicon (column 1, line 65 through column 2, line 12). To deposit tungsten silicide, tungsten hexafluoride and dichlorosilane are utilized (column 3, lines 44 through 49).

Koyama et al. disclose depositing tungsten silicide by reducing tungsten hexafluoride with dichlorosilane. The film is deposited at higher temperatures than when using silane. The resultant silicide has lower fluorine content which lowers stress variation during thermal treatment. The properties of the silicide so-produced make the polycide desirable for use

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as an electrode on a tunnel oxide as a gate. Such electrodes are described as useful in extending the endurance of EPROM's.

We have relied on the translation of Koyama et al. attached to appellants' brief as "prior art" under 35 U.S.C. § 102(a).

We recognize that appellants have characterized the article in their brief as being an article "by the inventor" (page 5 of appellants' brief). However, the inventive entity in the involved application is Yasuhiro Koyama and Hiroshi Ishihara. The authors of the article are Yasuhiro Koyama, Ryouzo Inoue, Jun Kudo and Hibou Shibayama. Thus, the authors of the article are "others" in terms of 35 U.S.C. § 102(a).⁶

We are not unmindful that Koyama et al. have made a claim for priority under 35 U.S.C. § 119 based on their earlier filed Japanese application which bears a filing date of September 19, 1991, which is prior to the publication date of the Koyama et al. article. However, an earlier filed foreign

⁶ 35 U.S.C. § 102(a) - "A person shall be entitled to a patent unless- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent,..." (1998).

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patent application must comply with the requirements of 35 U.S.C. 112, first paragraph, if the later filed U.S. application claiming the same invention as in the foreign application is to be accorded benefit under 35 U.S.C. § 119. In re Gostelli, 872 F.2d 1008, 1011, 10 USPQ2d 1614, 1616 (Fed. Cir. 1989); Vogel v. Jones, 486 F.2d 1068, 1075, 179 USPQ 425, 431 (CCPA 1973); Kawai v. Metlesics, 480 F.2d 880, 887-89, 178 USPQ 158, 164-65 (CCPA 1973). The written description requirement of 35 U.S.C. 112, first paragraph, is separate from the enablement requirement found in the same provision of 35 U.S.C. 112. In re Wilder, 736 F.2d 1516, 1520, 222 USPQ 369, 372 (Fed. Cir. 1984).

While appellants have filed the certified copy of their priority application required by 35 U.S.C. § 119(b), they have not supplied a sworn translation of the document which the statute also permits the Commissioner of Patents and Trademarks to require. See also 37 C.F.R. § 1.55(a), last sentence. Suffice it to say that without the translation, it is impossible to determine if the foreign application complies with the requirements of 35 U.S.C. § 112. Accordingly, on this record, we have not accorded appellants the benefit of

their earlier filed Japanese application and we have treated the article as prior art under 35 U.S.C. § 102(a).

THE REJECTION

As we have stated above, the claimed method differs from the admitted prior art by using dichlorosilane in place of silane. However, each of Hillman, Price'373, Price'474 and Koyama et al. teaches that dichlorosilane has been used in the manufacture of semiconductor devices for reducing tungsten hexafluoride to form tungsten silicide. The art recognizes certain process advantages in using dichlorosilane rather than silane. For example, Hillman discloses that using dichlorosilane results in cleaner deposition chambers. Price'343 discloses the use of dichlorosilane to reduce tungsten hexafluoride to deposit tungsten silicide yields an efficient, rapid lay down of tungsten silicide. Price'474 discloses that by using dichlorosilane to lay down both polycrystalline silicon and tungsten silicide greater bonding strength is obtained between the polycrystalline silicon and the tungsten silicide. Additionally, the layers so-produced have a low resistivity after sintering. Koyama et al. teach the resistance of silicide layers is reduced by using

dichlorosilane instead of silane for reducing tungsten hexafluoride. Koyama et al. also recognize improvement in the life of the tunnel oxide by using dichlorosilane, an improvement attributed to lower fluorine concentration.

From all of the above-noted, art recognized advantages, there would have been ample motivation to have used dichlorosilane in place of silane for reducing tungsten hexafluoride to prepare a tungsten silicide layer in a floating gate electrode. We realize that not every reference on which we have relied uses dichlorosilane for the same purpose that appellants use dichlorosilane. Nonetheless, each reference relied on does teach that dichlorosilane reduces tungsten hexafluoride to tungsten silicide. It is by now well-settled that all that is required to establish a *prima facie* case of obviousness is some motivation in the prior art to do what appellants have done, coupled with a reasonable expectation of success.

We are satisfied that the skilled chemical engineer, versed in the art of semiconductor manufacture, would have

used dichlorosilane instead of silane to reduce tungsten hexafluoride, motivated by the various advantages described by the art on which we rely. We also are satisfied because of the well-known chemistry involved in reducing tungsten hexafluoride with silanes, in general, that being so-motivated the person of ordinary skill would have expected to succeed in obtaining a tungsten silicide layer useful in the manufacture of various semiconductor devices, including floating gate electrodes.

With respect to the limitations of dependent claims 3, 5 and 7, we find that: Hillman in the examples and at column 4, lines 27 through 39; Price'343 at column 9, lines 5 through 16; Price'474 at column 3, lines 44 through 49; and Koyama et al. in their disclosure that higher temperatures are employed for reducing tungsten hexafluoride with dichlorosilane than with silane establish the reaction parameters and conditions claimed are well-known process variables in the CVD of tungsten silicide. Accordingly, the adjustment and selection of these variables would have been within the ordinary skill of a person in this art.

OTHER ISSUES

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In addition to the two Price patents disclosed in Hillman, there are disclosed, beginning at column 1, line 21 and concluding at column 1, line 45, what appear from the context of their description, numerous other references concerning the use of dichlorosilane in semiconductor manufacture. The appellants and the examiner should obtain copies of these references and consider them in the sense of their relevance under 35 U.S.C. §§ 102 and 103.

The Koyama et al. translation which was attached to appellants' brief appears from the table of contents to have been six pages long. Whether or not that was a reference to the length of the article in English is not clear. The text of the English translation attached to appellants' brief occupies one page with two pages of tables attached. If there are any additional pages of translation of the article, appellants are required in any further prosecution to forward them to the examiner for his consideration.

SUMMARY

The rejection of the claims under 35 U.S.C. § 112 is **reversed**. The rejection of the claims under 35 U.S.C. § 103

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is reversed. We have made a new ground of rejection under 37 C.F.R. § 1.196(b) and a recommendation under 37 C.F.R. § 1.196(c),

A statement pursuant to 37 C.F.R. § 1.196(c) has been made in this decision. 37 C.F.R. § 1.196(c) provides:

Should the decision of the Board of Patent Appeals and Interferences include an explicit statement that a claim may be allowed in amended form, appellant shall have the right to amend in conformity with such statement which shall be binding upon the examiner in the absence of new references or grounds of rejection.

This decision contains a new ground of rejection pursuant to 37 C.F.R. § 1.196(b) (amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)).

37 C.F.R. § 1.196(b) provides that, "A new ground of rejection shall not be considered final for purposes of judicial review."

37 C.F.R. § 1.196(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new

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ground of rejection to avoid termination of proceedings

(§ 1.197(c)) as to the rejected claims:

(1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner. . . .

(2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record. . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

REVERSED

37 C.F.R. 1.196(b)

37 C.F.R. 1.196(c)

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Administrative Patent Judge)
)
)
)
) BOARD OF PATENT
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